WHAT IS CLAIMED IS:

1. A capacitor apparatus comprising:

a first semiconductor wafer having a top surface coated with a dielectric material and having disposed on said dielectric material a highly doped semiconductor first plate region surrounded by a highly doped first peripheral rim,

a second wafer having a dielectrically isolating top surface and having disposed on said top surface a second highly doped semiconductor plate region surrounded by a highly doped second peripheral rim, with said rim of said second wafer isolated from said second plate by a peripheral moat providing electrical isolation between said second plate and said second rim,

said first and second wafers bonded together at said rims to form a capacitor having said first and second plates spaced apart by a distance determined in part by the height of one of said rims.

2. The capacitor apparatus according to claim 1 wherein said first wafer has a recessed area on a bottom surface, said recessed area positioned with respect to said first plate to allow said first plate to deflect upon application of a force to said recessed area, whereby the value of capacitance changes with respect to said deflection and therefore, according to the magnitude of said force.

3. The capacitor apparatus according to claim 1 further comprising a first aperture located on said second wafer and directed from a top to bottom surface to

communicate with said bonded rims, said aperture filled with a conductive material to form a first contact for said capacitor,

a second aperture located on said second wafer and directed from said top to said bottom surface to contact said second plate, said second aperture filled with a conductive material to form a second contact for said capacitor.

4. The capacitor apparatus according to claim 2 further comprising,

a spiral conductor disposed on the bottom surface of said second wafer, said inductor having first and second terminals located for connection to said first and second capacitor contacts to form a resonant circuit providing a frequency output proportional to said applied force.

5. The capacitor apparatus according to claim 1 wherein said first and second wafers are bonded together by a fusion bond.

6. The capacitor apparatus according to claim 1 wherein said first wafer is an N-type silicon wafer having a coating of silicon dioxide.

7. The capacitor apparatus according to claim 6 wherein said highly doped regions are P+ diffused regions.

8. The capacitor apparatus according to claim 4 wherein said inductor is a metal spiral deposited on said second wafer by RF sputtering or other deposition means.

9. The capacitor apparatus according to claim 1 wherein said second wafer is a Pyrex glass wafer.

10. The capacitor apparatus according to claim 1, wherein said second wafer is an N-type silicon wafer with said dielectrically isolating top surface being a layer of silicon dioxide.

11. The capacitor apparatus according to claim 4 further including means for hermetically sealing said resonant circuit in a housing.

12. The capacitor apparatus according to claim 1 wherein said first and second plate regions are relatively congruent.

13. The capacitor apparatus according to claim 1 wherein said rim of said second wafer is higher than said second plate area.

14. The capacitor apparatus according to claim 1 wherein said rim of said second wafer is the same height as said second plate area.

15. The capacitor apparatus according to claim 1 wherein said first plate region is generally rectangular in shape and having an extending tab on one side.

16. The capacitor apparatus according to claim 15 wherein said second plate region is generally rectangular in shape and having an extending tab on one side and is relatively congruent to said first plate region when said extending tabs facing each other.

17. The capacitor apparatus according to claim 16 wherein said extending tab of said second plate region is a contact tab to provide a contact area for said second plate region.

18. The capacitor apparatus according to claim 1 wherein the height of said first rim determines the spacing between said first and second plate regions and, therefore the magnitude of said capacitor.

19. The capacitor apparatus according to claim 1 wherein the height of said second rim determines the spacing between said first and second plate regions and, therefore, the magnitude of said capacitor.

20. The capacitor apparatus according to claim 1 wherein said highly doped semiconductor first plate and said first rim are disposed on said dielectric material by a fusion bond.